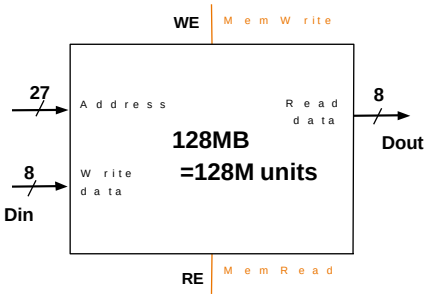
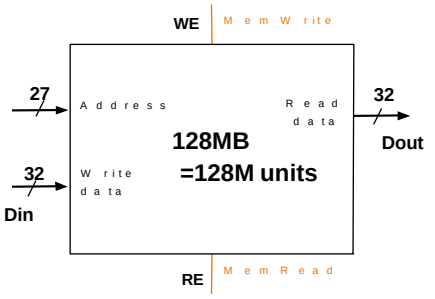
Main Memory Specification: Example 1

- Provide inputs and outputs of 128MByte memory with 8-bit read/write operations and byte addressability.



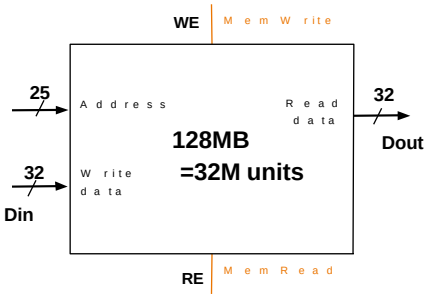
Main Memory Specification: Example 2

- Provide inputs and outputs of 128MByte memory with 32-bit read/write operations and byte addressability.



Main Memory Specification: Example 3

- Provide inputs and outputs of 128MByte memory with 32-bit read/write operations and 32-bit addressability.

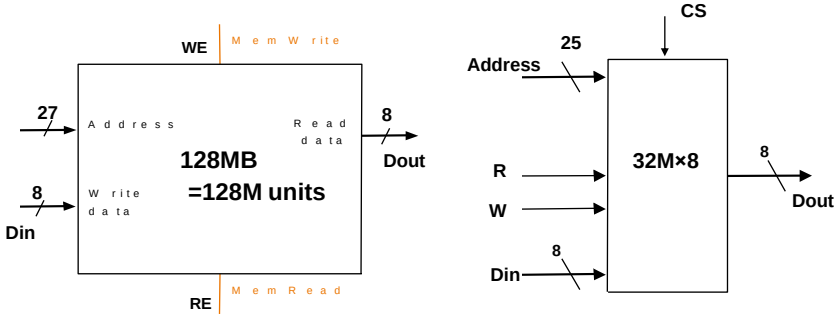


Steps in Memory Design

1. determine inputs and outputs for the memory to be designed and for the memory chips used;
2. determine number of memory chips needed;
3. determine number of memory chips in each set; a number of Dout and/or Din lines in the set should be identical to number of Dout and/or Din lines in the memory;
4. determine number of sets;
5. allocate sufficient number of memory address lines to select each of sets: those are the most significant address lines
6. allocate next set of memory address lines as inputs to all memory chip address lines;
7. If the number of bits in read/write operations equals the number of bits in addressability, then all memory address lines are used up in steps 5 and 6.
8. When condition in 7 is not satisfied → go to slide 24
9. Connect Din and Dout lines of memory and chips

Memory Design: Example 1

- Design 128MByte memory using 32M*8 chips, with 8-bit read/write operations and byte addressability.



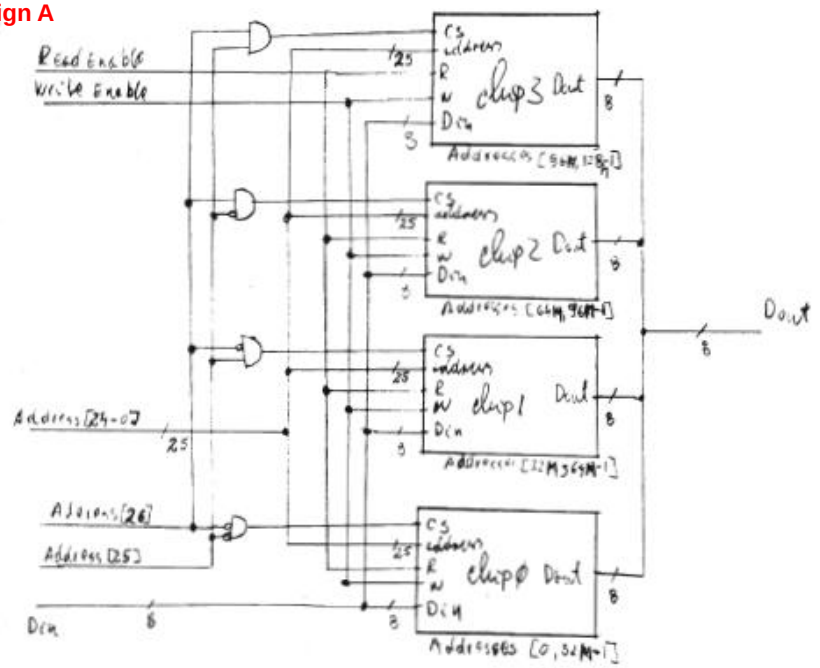
Number of chips needed: 4

Number of chips per set: 1

Number of sets: 4

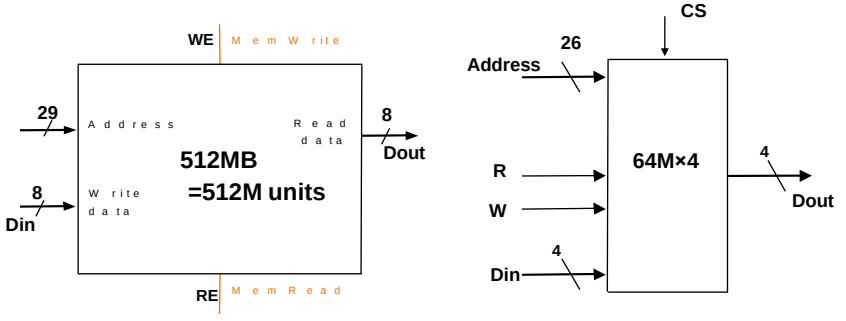
For the complete design see Design A.

Design A



Memory Design: Example 2

- Design 512MByte memory using 64M*4 chips, with 8-bit read/write operations and byte addressability.



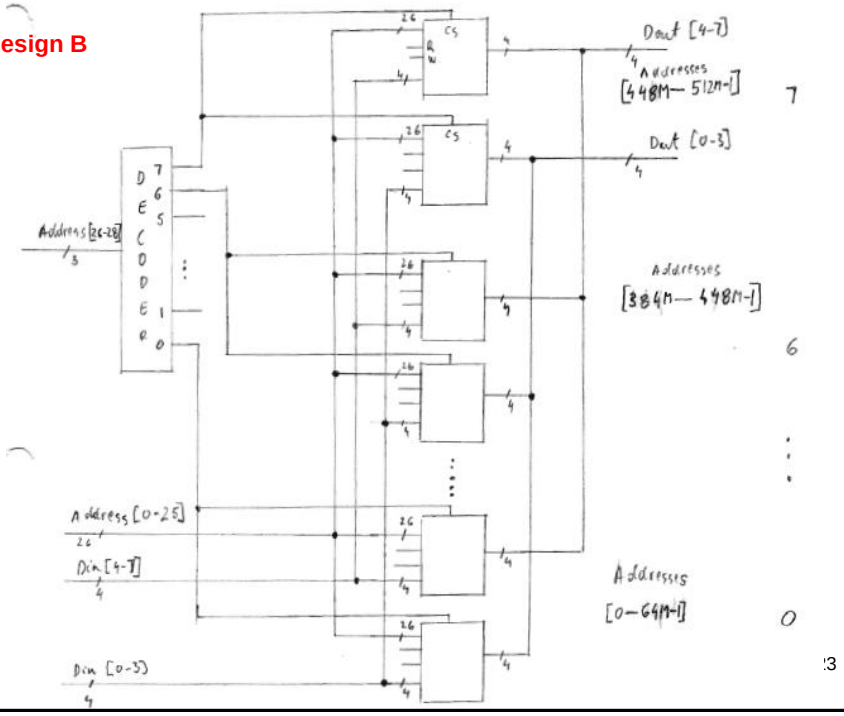
Number of chips needed: 16

Number of chips per set: 2

Number of sets: 8

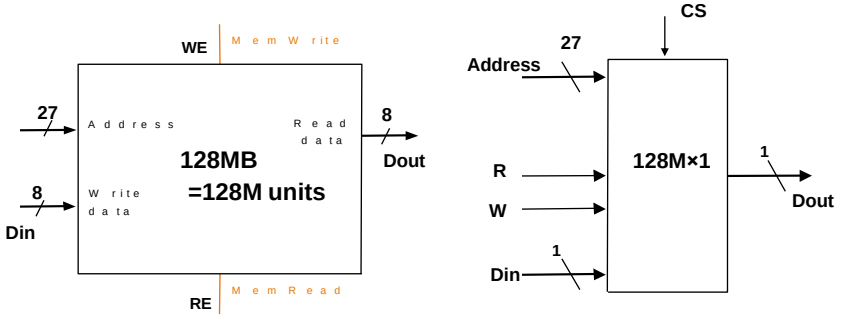
For the complete design see Design B.

Design B



Memory Design: Example 3

- Design 128MByte memory using 128M*1 chips, with 8-bit read/write operations and byte addressability.



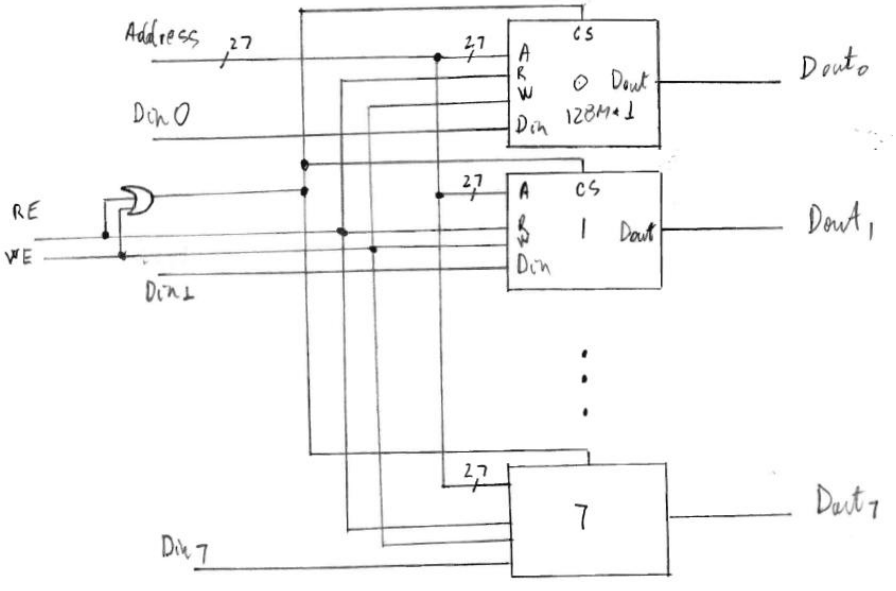
Number of chips needed: 8

Number of chips per set: 8

Number of sets: 1

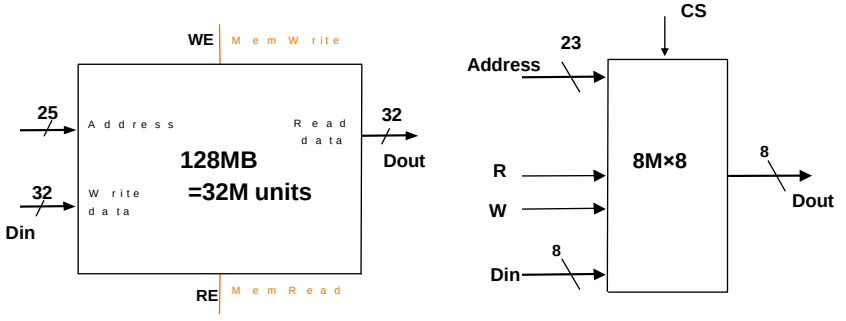
For the complete design see Design C.

Design C



Memory Design: Example 4

- Design 128MByte memory using 8M*8 chips, with 32-bit read/write operations and 32-bit addressability.



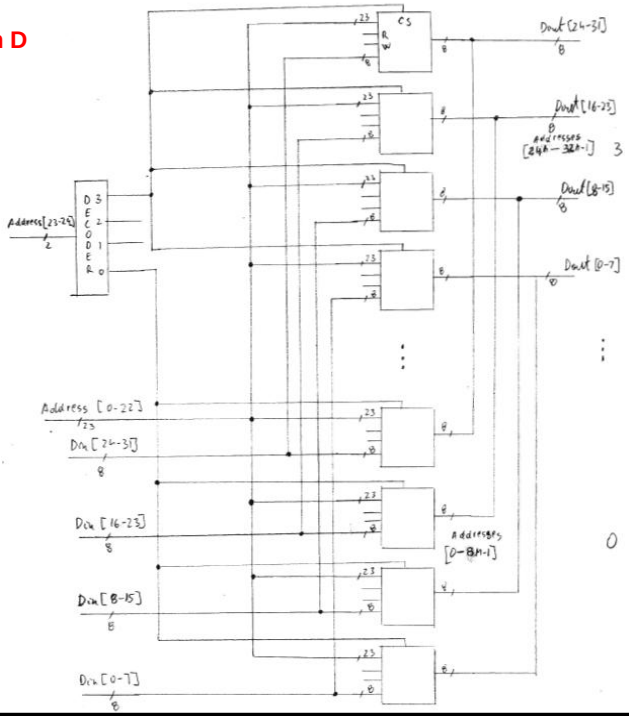
Number of chips needed: 16

Number of chips per set: 4

Number of sets: 4

For the complete design see Design D.

Design D

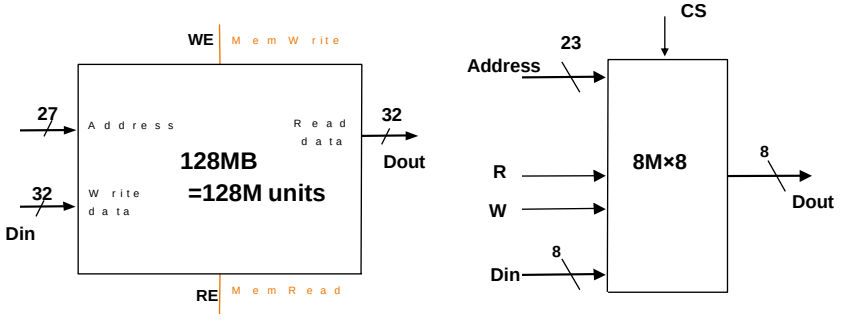


Steps in Memory Design (continued)

- This is the second part of step 7 in “Steps in Memory Design” slide:
  - when the number of bits in read/write operations is greater than the number of bits in addressability, then some lowest order memory address lines are not used
  - if the width of read/write operations is twice that of addressability then the least significant memory line is unused,
  - if the width of read/write operations is 4 times greater than the number of bits in addressability then the two least significant memory lines are unused, etc.
- Note, it doesn’t make sense to have the width of read/write operations smaller than addressability.

Memory Design: Example 5

- Design 128MByte memory using 8M*8 chips, with 32-bit read/write operations and 8-bit (byte) addressability.

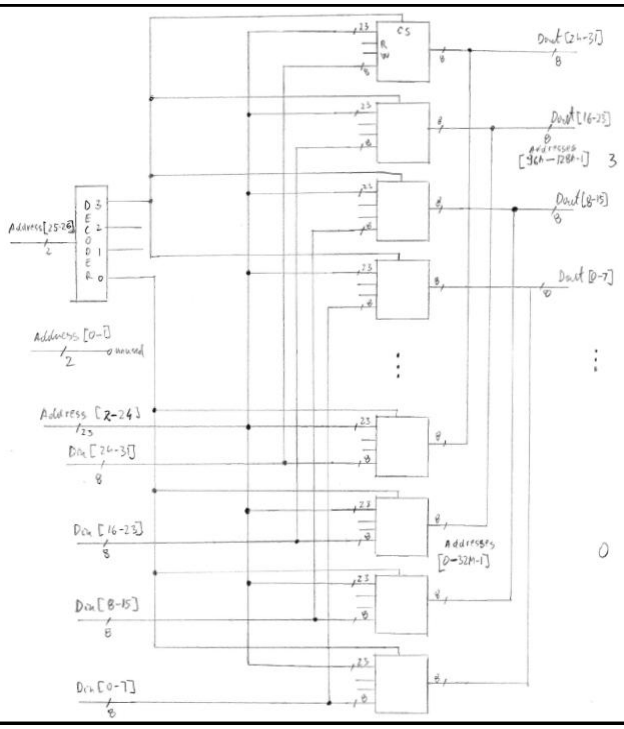


Number of chips needed: 16

Number of chips per set: 4

Number of sets: 4

For the complete design see Design E.


CS
Dout [24-31]
Dout [16-23]
Dout [8-15]
Dout [0-7]
Address [25-26]
DECODER
Address [0-1]
unused
Address [2-24]
Din [24-31]
Din [16-23]
Din [8-15]
Din [0-7]
Addresses [0-32M-1]
Addresses [96M-128M-1]
3
0