

Radu Teodorescu

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CURRENT POSITION ♦ **The Ohio State University** — Department of Computer Science and Engineering
Assistant Professor

EDUCATION ♦ **University of Illinois at Urbana-Champaign (UIUC)**, Urbana, IL
Ph.D. in Computer Science, August 2008
Thesis: *Techniques to Mitigate Parameter Variation*
Advisor: Josep Torrellas

♦ **University of Illinois at Urbana-Champaign (UIUC)**, Urbana, IL
M.S. in Computer Science, May 2005
Thesis: *Prototyping Architectural Support for Program Rollback Using Programmable Logic*

♦ **Technical University of Cluj-Napoca**, Romania
Dipl. Eng. in Computer Science, June 2002

AWARDS AND HONORS ♦ **W. J. Poppelbaum Award** - 2008
Awarded by the UIUC Computer Science Department to a graduate student in computer architecture, based on academic merit and creativity.

♦ **Intel Foundation Ph.D. Fellowship Award** - 2007–2008

♦ **David J. Kuck Outstanding Master's Thesis Award** - 2006
Awarded by the UIUC Computer Science Department to one Master's Thesis every year, based on quality and impact.

♦ **Romanian State Fellowship** - 1998–2002

♦ **Romanian State Scholarship** - 1997–1998

RESEARCH INTERESTS Computer architecture, multicore and parallel architectures, support for software debugging. Nanoscale technology scaling, reliability, variability and power management.

PUBLICATIONS TECHNOLOGY SCALING AND VARIABILITY

- [1] **Radu Teodorescu** and Josep Torrellas, *Variation-Aware Application Scheduling and Power Management for CMPs*, International Symposium on Computer Architecture (**ISCA**), June 2008.
- [2] **Radu Teodorescu**, Jun Nakano, Abhishek Tiwari and Josep Torrellas, *Mitigating Parameter Variation with Dynamic Fine-Grain Body Biasing*, International Symposium on Microarchitecture (**MICRO**), pages 27-39, December 2007 (20% acceptance rate).
- [3] Smruti R. Sarangi, Brian Greskamp, **Radu Teodorescu**, Jun Nakano, Abhishek Tiwari and Josep Torrellas, *VARIUS: A Model of Parameter Variation and Resulting Timing Errors for Microarchitects*, IEEE Transactions on Semiconductor Manufacturing (**IEEE TSM**), February 2008.
- [4] **Radu Teodorescu**, Brian Greskamp, Jun Nakano, Smruti R. Sarangi, Abhishek Tiwari and Josep Torrellas, *VARIUS: A Model of Parameter Variation and Resulting Timing Errors for Microarchitects*, Workshop on Architectural Support for Gigascale Integration (**ASGI**), in conjunction with ISCA, June 2007.

MULTICORE SOFTWARE DEBUGGING

- [5] Pin Zhou, **Radu Teodorescu** and Yuanyuan Zhou, *HARD: Hardware-Assisted Lockset-based Race Detection*, International Symposium on High-Performance Computer Architecture (**HPCA**), pages 121–132, February 2007 (14% acceptance rate).
- [6] S. Chen, B. Falsafi, P. B. Gibbons, M. Kozuch, T. C. Mowry, **R. Teodorescu**, A. Ailamaki, L. Fix, G. R. Ganger, B. Lin, S. W. Schlosser, *Log-Based Architectures for Continuous Monitoring of Deployed Code*, Workshop on Architectural and System Support for Improving Software Dependability (**ASID**), in conjunction with ASPLOS, October 2006.
- [7] **Radu Teodorescu**, Jun Nakano, and Josep Torrellas, *SWICH: A Prototype for Efficient Cache-Level Checkpointing and Rollback*, **IEEE Micro Magazine**, pages 28–40, September–October 2006.
- [8] **Radu Teodorescu** and Josep Torrellas, *Empowering Software Debugging Through Architectural Support for Program Rollback*, Workshop on the Evaluation of Software Defect Detection Tools (**BUGS**), in conjunction with PLDI, June 2005.
- [9] **Radu Teodorescu** and Josep Torrellas, *The Design Complexity of Program Undo Support in a General-Purpose Processor*, Workshop on Complexity-Effective Design (**WCED**), in conjunction with ISCA, June 2005.
- [10] **Radu Teodorescu** and Josep Torrellas, *Prototyping Architectural Support for Program Rollback Using FPGAs*, Symposium on Field-Programmable Custom Computing Machines (**FCCM**), pages 23–32, April 2005 (28% acceptance rate).
- [11] **Radu Teodorescu** and Josep Torrellas, *Prototyping Architectural Support for Program Rollback: An Application to Software Debugging*, Workshop on Architecture Research Using FPGA Platforms (**WARFP**), in conjunction with HPCA, February 2005.

MEDICAL IMAGE PROCESSING AND STRUCTURED REPORTING

- [12] S. Nedevschi, **R. Teodorescu**, Z. Gyongyi, S. Nedevschi Jr., A. Leuca, and D. Olinic, *Integrated Medical Imaging Environment*, International Conference on Automation, Quality and Testing, May 2002.
- [13] S. Nedevschi, Z. Gyongyi, **R. Teodorescu**, S. Nedevschi Jr. and D. Olinic, *Distributed System for Medical Image Acquisition, Processing, Storage, and Retrieval*, First RoEduNet Conference, April 2002.
- [14] S. Nedevschi, I. Salomie, Z. Gyongyi, **R. Teodorescu**, S. Nedevschi Jr. and D. Olinic, *Retrieval of DICOM Ultrasound Images Based on Structured Medical Description*, International Conference on Emerging Telecommunications Technologies and Applications, October 2001.
- [15] S. Nedevschi, Z. Gyongyi, **R. Teodorescu**, S. Nedevschi Jr. and D. Olinic, *E-environment for Medical Image Processing*, Electronic Business on the Internet, October 2001.
- [16] S. Nedevschi, D. Olinic, Z. Gyongyi, **R. Teodorescu** and S. Nedevschi Jr., *Feature-based Retrieval of Echocardiographic Images using DICOM Structured Reporting*, IEEE Computers in Cardiology, September 2001.

THESES

- ◇ **Radu Teodorescu**, *Prototyping Architectural Support for Program Rollback Using Programmable Logic*, University of Illinois at Urbana-Champaign, **Master's Thesis**, May 2005. Advisor: Josep Torrellas
- ◇ **Radu Teodorescu**, *DICOM Compliant Structured Reports - Encoding and Communication*, Technical University of Cluj-Napoca, **Diploma Thesis**, June 2002. Advisor: Sergiu Nedevschi

RESEARCH EXPERIENCE ◇ **University of Illinois at Urbana-Champaign**, Research Assistant, (2002–present)

ARCHITECTURAL TECHNIQUES FOR TOLERATING PARAMETER VARIATION

Parameter variation (the deviation of manufacturing process, voltage and temperature from nominal specifications) has a detrimental impact on processor frequency, power consumption and reliability. In this work, I developed architectural approaches to mitigate this impact. I proposed a novel technique based on the continuous adaptation of body bias voltages that can be applied at fine granularity within a chip [2]. This results in better frequency and power characteristics of processors affected by variation. I also worked on developing variation models that can be used in microarchitectural studies [3,4].

As a result of variation, identically designed cores in future chip multiprocessors will differ significantly in both static power consumption and maximum frequency. In such an environment, exposing this variation to the operating system can be beneficial. I proposed and evaluated a set of variation-aware application scheduling and power management algorithms aimed at saving power and improving performance [1].

ARCHITECTURAL SUPPORT FOR SOFTWARE DEBUGGING

I developed hardware support for low-overhead software bug characterization and graceful recovery which allows online debugging of production code. It is based on a hardware primitive that quickly rolls back long sections of code, using cache-level checkpointing. I designed, implemented and tested the first processor with software-controlled cache-level checkpointing and rollback support, in a fully functional FPGA implementation [10,11,9,8]. Parallel applications are especially hard to debug, because they are prone to synchronization bugs such as data races. Good software race detection tools, such as those using the Lockset algorithm, are slow. I worked on the first hardware implementation of the Lockset algorithm to exploit its race detection capabilities with minimum overhead [5].

◇ **Intel Research Pittsburgh**, Graduate Technical Intern, (Summer 2006)
Mentors: Mike Kozuch, Phillip Gibbons

In this work, I examined Log-Based Architectures as a potential solution for lifetime application monitoring [6]. In this framework, as an application executes on a chip multiprocessor, the hardware captures a log of the application's execution. Monitoring programs, which run on separate cores, read the log to check for software bugs. I designed and evaluated techniques for efficient representation, transport and control of the log data inside the chip multiprocessor and through the on-chip cache hierarchy.

◇ **Technical University of Cluj-Napoca, Romania**, Research Assistant, (1999–2002)

INTEGRATED MEDICAL IMAGING ENVIRONMENT

The project involved the development and management of a distributed medical application for storage, communication and retrieval of medical images and associated structured patient reports [12,13,14,15,16].

DESIGN AND IMPLEMENTATION OF A RISC MICROCONTROLLER

In this work, we built a simple RISC microcontroller in an FPGA. The project required design to specifications, VHDL and schematic implementation, extensive testing and machine-level programming.

TEACHING EXPERIENCE ◇ **University of Illinois at Urbana-Champaign**, Teaching Assistant, (Spring 2006, 2008)
CS533 - *Parallel Computer Architectures* - Advanced graduate level course on research issues in parallel architectures, with about 30 students.

TALKS AND DEMOS	<ul style="list-style-type: none"> ◇ Variation-Aware Application Scheduling and Power Management for Chip Multiprocessors, 35th International Symposium on Computer Architecture, Beijing, China, June 2008. ◇ Mitigating Parameter Variation with Dynamic Fine-Grain Body Bias, International Symposium on Microarchitecture, Chicago, December 2007. ◇ Mitigating Parameter Variation with Dynamic Fine-Grain Body Bias, Intel PhD Fellowship Forum, Hillsboro, Oregon, October 2007. ◇ Empowering Software Debugging Through Architectural Support for Program Rollback, Workshop on the Evaluation of Software Defect Detection Tools, in conjunction with PLDI 2005, Chicago, June 2005. ◇ The Design Complexity of Program Undo Support in a General-Purpose Processor, Workshop on Complexity-Effective Design, in conjunction with ISCA 2005, Madison, Wisconsin, June 2005. ◇ Prototyping Architectural Support for Program Rollback Using FPGAs, Illinois Department of Computer Science, Affiliates Conference, demo, Urbana, Illinois, April 2005. ◇ Prototyping Architectural Support for Program Rollback Using FPGAs, IEEE Symposium on Field Programmable Custom Computing Machines, Napa, California, April 2005. ◇ Prototyping Architectural Support for Program Rollback: An Application to Software Debugging, Workshop on Architecture Research Using FPGA Platforms, in conjunction with HPCA-11, San Francisco, February 2005. ◇ Building a Hardware Prototype for Thread Level Speculation using Programmable Logic, Siebel Center Open House, poster and demo, Urbana, Illinois, May 2004. ◇ Integrated Medical Imaging Environment, International Conference on Automation, Quality and Testing, Cluj-Napoca, Romania, May 2002.
SERVICE	<p>Reviewer for ISCA, MICRO, DSN, Transactions on Computers.</p> <p>Helped organize the SELSE 2 workshop at UIUC in April 2006.</p> <p>Helped with the IEEE MICRO Top Picks program committee meeting in October 2005.</p> <p>Helped organize the Siebel Center Open House at UIUC in May 2004.</p> <p>Member of the Semiconductor Research Corporation (SRC) and IEEE.</p>
GRADUATE LEVEL COURSES	<p>Computer Architecture, High Performance Computer Architecture, High Speed Parallel Systems, Dynamic Translation and Optimization, Compiler Construction, Fault Tolerant Systems, Advanced Operating System Design, High Performance Computer Networks, Combinatorial Algorithms, Reliable and Robust Software Systems</p>
STATUS	<p>Romanian citizen, on F1 student visa.</p>

- REFERENCES
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