

Research Interest

Microarchitecture (CPU/GPU) design for high-performance computing applications.

Education

PhD: The Ohio State University (OSU)	Columbus, OH
Major: Computer (Systems) Engineering	2010 - Current
Minors: Computer Architecture, Programming Languages	Expected Graduation: Early 2014
MSc: University of Tehran (UT)	Tehran, Iran
Major: Computer Architecture	2004 - 2007
BSc: Ferdowsi University of Mashhad (FUM)	Mashhad, Iran
Major: Computer Engineering	1999 - 2004

Publications

1. T. N. Miller, X. Pan, R. Thomas, **N. Sedaghati**, R. Teodorescu, *Booster: reactive core acceleration for mitigating the effects of process variation and application imbalance in low-voltage chips*, Int. Symposium on High-performance Computer Architecture (HPCA), 2012.
2. **N. Sedaghati**, R. Thomas, L. N. Pouchet, R. Teodorescu, P. Sadayappan, *StVEC: a vector instruction extension for high-performance stencil computation*, Int. Conference on Parallel Architectures and Compilation Techniques (PACT), pp. 276-287, 2011.
3. **N. Sedaghati**, M. N. Bojnordi, A. Hormati, S. M. Fakhraie, *An efficient and extendable modeling approach for VLIW DSP processors*, Springer-Verlag CCIS, no. 6, pp. 267-274, 2008.
4. **N. Sedaghati**, M. N. Bojnordi, S. M. Fakhraie, *MDST: multiprocessor DSP simulation toolkit for voice processing applications*, IEEE/ACM Int. Sym. on Modeling, Analysis, and Simulation of Computer and Telecommunication Systems (MASCOTS), pp. 173-179, 2007.
5. N. Honarmand, M. R. Javaheri, **N. Sedaghati**, A. A. Kusha, *Power efficient sequential multiplication using pre-computation*, IEEE Int. Symposium on Circuit and System (ISCAS), pp. 2709-2712, 2006.
6. M. N. Bojnordi, **N. Sedaghati**, O. Fatemi, M. R. Hashemi, *An efficient self-transposing memory structure for 32-bit video processors*, IEEE Asia Pacific Conf. on Circuits and Systems (APCCAS), pp. 1484-1487, 2006.
7. **N. Sedaghati**, S. Rahmanian, S. M. Fakhraie, *Hardware implementation analysis for digital filters*, IEEE Iranian Conference on Electrical Engineering, 2006.
8. **N. Sedaghati**, *Micro-step driving for stepper motors: a case study*, Iranian Student Conference on Electrical Engineering, University of Tehran, 2006.

Research Experience

Graduate Research Assistant, CSE Department, The Ohio State University	2010 - Current
Architecture design for HPC applications, with emphasis on fused CPU-GPU architectures.	
Graduate Research Assistant, ECE Department, University of Tehran	2004 - 2007
Designed and developed a multi-core DSP simulator for high-performance voice processing	
Research Assistant, CE Department, Ferdowsi University of Mashhad	2002 - 2004
Designed and implemented a testing platform for small-size robots	

Teaching Experience

Graduate Teaching Assistant, ECE Department, North Carolina State University	2009 - 2010
Intro to computer systems (SP-2010), computer systems programming (FA-2009, SP-2010), DSP architecture (SP-2009).	
Graduate Teaching Assistant, ECE Department, University of Tehran	2005 , 2007
Custom implementation of DSP systems (SP-2007), digital logic design (SP-2005).	

Work Experience

Software System Administrator, University of Tehran e-Learning Center (UTEC)	2007 - 2008
Implemented a Linux-based backup-recovery system for the e-learning infrastructure.	
Hardware Engineer, SiNA Microelectronics Inc.	2005 - 2007
Designed and developed a VLIW DSP model for telecommunication applications.	

Research Projects

- New Vector Instruction Extension for Stencils** OSU - 2011
StVEC, an extension to the standard addressing mode of vector instructions, overcomes the performance limitation of current short-vector SIMD ISAs (e.g. SSE/AVX) for stencil computations.
- Data-dependence profiler on GCC for OpenMP parallel programs** NCSU - 2010
Can be added to the GCC compiler, profiler keeps track of the reads/writes to shared memory and maintains a data-dependence database for multi-threaded OpenMP applications.
- A multi-core DSP simulation toolkit for voice processing applications** UT - 2007
The toolkit implements an abstract C++ model of multiple DSP cores connected via a hierarchical bus to simulate data parallelism in multi-channel voice processing applications (i.e. in VoIP).
- A testing platform for small-size robots** FUM - 2004
The platform has circuitry to micro-step/drive the stepper motors, IR receive/transmit, run C51 micro-controller, and interface PC with RS-232 PC plus a software on PC to control the robot.

Work Projects

- An automated Linux-based backup-recovery system for a virtual university** UTEC - 2008
The software automates information gathering, backup and retrieval (on tape) from workstations/servers in a virtual university's computer center using native Linux scripting languages.
- HDL modeling and synthesis of a DSP processor (similar to TI C62xx)** SiNA - 2006
The work includes design and implementation of synthesizable Verilog plus abstract C++ models for an 8-way VLIW processor that can be integrated as a DSP core in telecommunications chips.

Course Projects

- LISP Interpreter** OSU - 2010
The interpreter, implemented with Java, scans a LISP program, parses the generated tokens (on demand), evaluates the given input and generates the output LISP program, as an S-expression.
- A user-level threading library** NCSU - 2010
A Linux-based user-level thread management library that mimics Pthread APIs, such as thread creation, join, yield, identification, etc. It is implemented using native setjmp/longjmp functions.
- Compiler back-end (including classic code generation and optimization algorithms)** NCSU - 2009
AST to assembly including dataflow analysis (e.g. liveness), classical scalar optimizations (e.g. DCE), and code scheduling (both cyclic (loop) and acyclic scheduling plus register allocation).
- Modeling a super-scalar processor (cache, branch-predictor, dynamic scheduler)** NCSU - 2009
High-level C++ models for: 1- a generic cache (L1 and L2) with hardware prefetch, 2- branch predictors (i.e. gshare, bimodal and hybrid), 3- dynamic out-of-order instruction scheduler.
- A low-power circuit for sequential multiplication** UT - 2005
A sequential multiplier that reduces dynamic (switching) power by pre-computing inputs and eliminating trivial and unnecessary partial values (e.g. zeros) from shift-and-add operations.
- Custom circuit design for IIR digital filters** UT - 2005
Verilog/Matlab modeling of digital IIR filter with combinational and sequential circuits to measure the accuracy (quantization overhead), performance and also power consumption.
- HDL modeling/synthesis of 5-stage MIPS pipeline** UT - 2004
A 5-stage in-order MIPS pipeline is modeled and synthesized for custom ASIC chips. This includes Verilog modeling, pre- and post-synthesis simulation plus spice circuit simulation using HSPICE.

Skills

Programming Languages

Parallel (OpenMP, MPI, Pthread), C/C++/Java, Assembly (x86, TI's C6x), GPU (CUDA, OpenCL), \LaTeX

Operating Systems

Linux, Microsoft Windows.

Hardware Description Languages

Verilog, VHDL, SystemC

Engineering Tools

SimpleScalar, CCStudio, Matlab, FPGA-ASIC CAD (ISE, Modelsim), NS-2, SESC, GCC, GDB.

Relevant Graduate Courses

CSE Department, The Ohio State University

2010 - Current

High-performance computing, programming languages, distributed operating systems, algorithm design, computability and complexity, advanced computer architecture, software dependability and security, low-power microprocessor architectures, compiler design and implementation.

ECE Department, North Carolina State University

2009 - 2010

Computer organization and design, parallel computer architecture, advanced micro-architecture, code generation and optimization, embedded System Design, operating systems principles.

ECE Department, University of Tehran

2004 - 2007

Advanced computer architecture, VHDL, advanced VLSI, low-power integrated circuits, custom design of DSP systems, computer arithmetic algorithms, parallel processing.

References

Available upon request