

CSE 775  
Autumn 2008  
Homework #4

Instructor: Panda

Due: Friday, 5th December

1. (20 points) Consider a memory system with a capacity of  $2^{28}$  bytes. The processor system has a 1024-word cache with 8-word (each word being 4 bytes) block size.

For the following four cache organizations, determine how many bits are used for tag, index, and block offset, respectively.

- (a) direct-mapped
  - (b) 4-way set-associative
  - (c) 8-way set-associative
  - (d) fully set-associativity
2. (10 + 50 = 60 points)

Consider the following MIPS program. All specified values (address and data) are in decimal.

```

                DADD    r1,r0,r0
                DADDI   r2,r0, # 256
X1:            LD      r3, 1000(r1)
                LD      r4, 1064(r1)
                DADD    r3,r3,r4
                SD      1000(r1),r3
                DADDI   r1,r1, # 8
                DSUBI   r2,r2, # 1
                BNEZ    r2,X1
                NOP
```

- (a) How many memory read and write references are used for *data* access in executing the above loop?
- (b) For the following five cache organizations, determine the percentage of read hit, read miss, write hit, and write miss memory references for data accesses. Explain your answers.
  - i. Direct-mapped, write-through, no-write-allocate, data cache size = 8 words, block size = 2 words.
  - ii. Direct-mapped, write-through, no-write-allocate, data cache size = 16 words, block size = 2 words.
  - iii. Direct-mapped, write-through, no-write-allocate, data cache size = 32 words, block size = 2 words.
  - iv. Direct-mapped, write-through, no-write-allocate, data cache size = 32 words, block size = 4 words.
  - v. Fully-associative, write-through, no write-allocate, FIFO replacement, data cache size = 32 words, block size = 2 words.

3. (20 points) Consider an 8-way interleaved memory organization. Each memory bank is 1-word wide. The bus between the cache and interleaved memory is 1-word wide. The cost for putting an address is 1 clock cycle. The cost for accessing the data is 6 clock cycles. It takes one clock cycle to transfer 1 word between the cache and memory.

For the cache organizations in problems #2.b (i, ii and iii), determine the overall memory penalty by taking into account read miss and writes.