CSE 775: Computer Systems Architecture
Autumn 2008
Homework #2

Instructor: Panda Due: Wednesday, 22nd October

1. (25 points) Consider the instruction mix for five different benchmarks (gap, gcc, gzip, mcf and perlbmk), as shown in Figure B.27.

   (a) For each of these benchmarks, group these instructions into three major categories (memory-oriented, alu-oriented and control-oriented) and determine their frequencies.

   (b) As an architect, you are designing a processor with the following individual CPIs for the three instruction classes (memory - 6 cycles, alu - 4 cycles and branch - 5 cycles). Determine the effective CPIs for each of these benchmarks. Identify the two benchmarks which will run fastest and slowest on this processor.

   (c) Your manager asks to propose enhancements to the processor design so that the benchmark running slowest on this processor can be accelerated by 25% or more. Indicate two methods by which you can achieve such an enhancement. Show the reasoning.

2. (35 points) Consider the following MIPS code sequence. For each of these instructions, determine the appropriate instruction type to be used for encoding. Assuming the code sequence starts at memory address 1000(Hex), show how the instructions are encoded. Indicate the values of the main fields for each of the instructions and their corresponding memory addresses where they are stored.

```
        DADDI   R1, R0, #32
        DADD    R2, R0, R0
Loop:   L.D     F2, 1000(R2)
        L.D     F3, 2000(R2)
        ADD.D   F4, F2, F3
        L.D     F6, 3000(R2)
        MUL.D   F7, F4, F6
        S.D     F7, 4000(R2)
        DADDI   R2, R2, #4
        DSUB    R3, R1, R2
        BNEZ    R3, Loop
```

3. (15 points) Consider adding a new addressing mode to MIPS for ALU operations so that instructions like *DADD Rx, Rx, 100(Ry)* can be executed. Such operations will make MIPS look like a CISC processor where one of the operand is coming from memory.

   Specify a suitable instruction format to encode instructions using this new mode. (You can ignore the 'function' field for this enhancement.) What is the maximum *range* of offset that can be specified in this addressing mode? Indicate if any of the existing format can be used for encoding it and show how to use it.

4. (25 points) Consider a 7-stage pipeline sequence for a processor (IF, ID, EX1, EX2, MEM, EX3 and WB). The overhead for these seven stages are as follows: 5nsec, 4nsec, 6nsec, 6nsec, 8 nsec, 6nsec and 5nsec. There are three major types of instructions (I, II and III). In a non-pipelined design they use the following stages: I (IF, ID, EX1, MEM and WB), II (IF, ID, EX1, EX2, MEM and WB) and III (all stages). Let the frequencies of these instruction types be as follows: I (30%), II (40%) and III (30%).

   (a) Assuming 1000 instructions in a program, determine how much time will it take to execute the program on a non-pipelined processor with the above 7 stages.

   (b) Consider pipelining the above design. Consider a latch overhead of 1 nsec. What should be the clock cycle time for the pipelined design?

   (c) How much time will the program with 1000 instructions take to execute on the pipelined processor? What will be the pipelined speedup?