

## Tentative Class Schedule

<u>Week</u>	<u>Topics</u>	<u>Readings from Text</u>
Sept 24	Introduction; Course Overview Technology Trends	1.1–1.3
Sept 29	Cost, Performance & Dependability Quantitative Principles of Computer Design Reading Assignment Classifying Instruction Set Architectures and Features	1.4–1.8 1.9 1.10–1.11 B.1–B.7
Oct 6	Role of Compilers and MIPS Architecture Basic Pipelining Hw#1 due (Oct 8)	B.8–B.9 A.1
Oct 13	Data and Control Hazards Pipelining Implementations and Multicycle operations	A.2 A.3–A.4
Oct 20	Multicycle operations Hw#2 due (Oct 20)	A.5
Oct 27	MIPS R4000 pipeline Crosscutting Issues in Pipelining Lab#1 due (Oct 27) MIDTERM (Oct 29)	A.6 A.7
Nov 3	Instructional-Level Parallelism Dynamic Scheduling and Branch Prediction	2.1–2.2 2.3–2.5
Nov 10	Hardware-based Speculation Advanced Techniques Lab#2 due (Nov 10)	2.6–2.7 2.8–2.10
Nov 17	Memory-Hierarchy Design and Caches Memory-Hierarchy Design and Caches Cache Optimizations Hw#3 due (Nov 19)	C.1 and 5.1 C.2 C.3 and 5.2
Nov 24	Virtual Memory Main Memory Design Issues	C.4 5.3
Dec 1	Overview of Interconnection Networks Overview of Multiprocessing Overview of Latest Multicore Processors Hw#4 due (Dec 1) Lab#3 due (Dec 3)	Appendix E 4.1
	FINAL Exam (Dec 8)	