Report on CSE 778

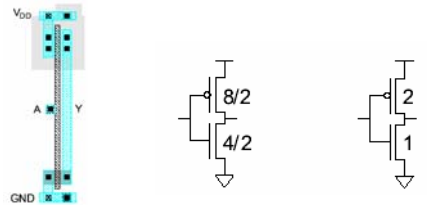
Computer-Aided Design and Analysis of VLSI Circuits

P. Sadayappan

Course Information

- Taught every Autumn, MWF 12:30-1:16; 4 credits
- Around 25 students, mix of CSE-UG/G, ECE-UG/G
  - AU04: 7 cse-ug, 9 cse-g, 4 ece-ug, 5 ece-g
- Course covers both "low-level" and "high-level" design (two separate graduate-level courses in ECE)
  - Low-level: Transistor-level design and layout; used for creating building blocks like adders, shifters, registers etc.
  - High-level: Hardware Description Language (Verilog); used for system design

Low-Level Design



- Topics:
  - CMOS circuit design techniques
  - Layout design, extraction
  - Effect of transistor size on performance
  - Simulation for functional testing and timing characterization

Coursework

- First half: Low-level design
  - 2 Labs, 2 HW's, 1 Design Project
  - Design project (individually done) emphasizes iterative design to achieve circuit performance goals
  - Use simple analytical model to develop initial design; implement circuit, create layout, extract and simulate to characterize performance; identify performance bottleneck and redesign; iterate several times till optimal performance is achieved.
  - Written Project Report describing initial design and documenting design iterations.
- Mid-term
- Second half: High-level design using HDL's
  - Group project (2 students): design/verification of simple system (e.g. Soda-machine controller; Digital alarm clock)
  - Group presentation (oral, ~ 20 minutes)

Capstone Criteria 1 & 2 & 3

- **Criteria 1 & 2**
  - Is at the senior level
  - Pre-requisites CSE 560, CSE 601, CSE 675, ECE 561
- **Criterion 3: Design component**
  - Design is a significant focus in course: 2 labs and 2 projects
  - Project 1 illustrates design iteration typical in industry

Criterion 4: Course Content

- Realistic constraints
  - Performance constraints
- Standards
  - Verilog HDL is an IEEE standard
  - Layout design rules
- Maintainability
  - Currently not emphasized in course; could look for ways of addressing this in future offerings

Criterion 5: Documentation

- Written project reports for project 1 & 2
- Project designs are documented in project reports, but no specified structure for the documentation
  - Ad hoc, using mix of schematics, English descriptions, source code fragments, annotated simulation output etc.
  - Would be desirable to provide greater structure for design documentation

Criterion 6: Oral Presentation

- Each group makes an oral presentation (about 20 minutes; 10 minutes by each partner)
  - Topic is either Design Project 2, or
  - Any other pre-approved topic pertaining to course matter
- Feedback & Peer Evaluation
  - Students fill out feedback forms
  - Good attendance (offered a small amount of extra credit)
- Presentation on Design Project vs. Other topics
  - Few groups chose to present their Project 2 design
  - Alternative topic presentations were much more interesting
    - e.g. Pentium Architecture; Itanium Architecture; Phase-Locked Loops; Commercial CAD Tools; CAD Synthesis

Criteria 7: Teamwork

- Project 2 was done in 2-person teams
- Oral presentation required presentation by both team members
- Team choice was left to students
  - Considered mixing CSE and ECE, but class was not quite balanced in count
- Nothing formalized regarding work partitioning and team interaction; nothing explicitly reported
  - For project 2, the overall effort is definitely reduced by partitioning design work: teams divided up work by dividing up component modules of design
  - For oral presentation, typically two coordinated and linked presentations

Criterion 8: Course-size

- Cap: 30
- Enrolment over last few years has been around 25