

CSE 775
Spring 2006

Homework 3

Instructor: Lauria

1. (20 points) Consider a memory system with a capacity of 2^{32} bytes. The processor system has a 4096-byte cache with 32-byte block size. For the following four cache organizations, determine how many bits are used for tag, index, and block offset, respectively.
 - (a) direct-mapped
 - (b) 4-way set-associative
 - (c) 32-way set-associative
 - (d) fully set-associativity

2. (80 points) Consider the execution of the following loop. Each element of array A and B is double-word-oriented (i.e., 8 bytes each). Assume array A is stored starting with byte address 1000 (in hexadecimal) and array B with byte address 8000 (in hexadecimal)

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for i:=0 to 127 do
  A[i] = A[i]+B[i]
```

 - (a) How many memory read and write references are used for data access in executing the above loop?

 - (b) Consider a 128-byte data cache. Assume the assembly-level instructions are organized in such a manner that A[i] is loaded first and then B[i]. For the following four data cache organizations, determine the number of read hit, read miss, write hit, and write miss memory references (accesses). Explain your answers.
 - i. Direct-mapped, write-through, no-write-allocate, block size = 32 bytes.
 - ii. Direct-mapped, write-back, write-allocate, block size = 32 bytes.
 - iii. 2-way set-associative, write-through, no-write-allocate, FIFO replacement, block size = 32 bytes.
 - iv. Fully-associative, write-through, no-write-allocate, FIFO replacement, block size = 16 bytes.

Note: There is no need to use any tool. For this small program and cache size, one can use a *pen and paper simulation* of the cache behavior.